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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 : G09G 1/16 — A1

(11) International Publication Number: **WO 97/06523**

(43) International Publication Date: 20 February 1997 (20.02.97)

(21) International Application Number: PCT/US96/12829

(22) International Filing Date: 5 August 1996 (05.08.96)

(30) Priority Data:
08/512,574 8 August 1995 (08.08.95) US

(71) Applicant: CIRRUS LOGIC, INC. [US/US]; Legal Dept. M/S 521, 3100 West Warren Avenue, Fremont, CA 94583-6423 (US).

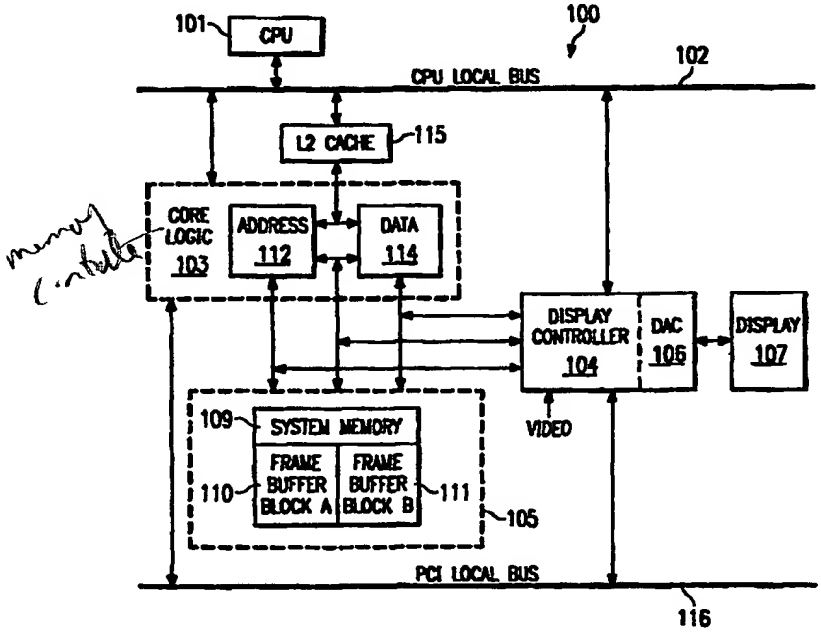
(72) Inventor: RAO, G., R., Mohan; 5723 Covehaven Drive, Dallas, TX 75252 (US).

(74) Agents: SHAW, Steven, A. et al.; Cirrus Logic, Inc., Legal Dept. M/S 521, 3100 West Warren Avenue, Fremont, CA 94538 (US).

(81) Designated States: JP, KR, European patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Published
*With international search report.*
*Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.*

(54) Title: UNIFIED SYSTEM/FRAME BUFFER MEMORIES AND SYSTEMS AND METHODS USING THE SAME




(57) Abstract

A processing system (100) includes a unified memory system (105) having a system memory area (109) and a plurality of frame buffer areas (110/111). A central processing unit (101) has within its address space unified system memory (105) and is operable to update display data in a first selected one from the frame buffer areas (110/111) while display data from a second selected one of the frame buffer areas (110/111) provides data for refresh of a display screen of an associated display device.

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# UNIFIED SYSTEM/FRAME BUFFER MEMORIES AND SYSTEMS AND METHODS USING THE SAME

## TECHNICAL FIELD OF THE INVENTION

The present invention relates in general to data processing systems including display subsystems and in particular to unified system/frame buffer memories and systems and methods using the same.

## BACKGROUND OF THE INVENTION

A typical processing system with video/graphics display capability includes a central processing unit (CPU), a display controller coupled with the CPU by a CPU local bus (directly and/or through core logic), a system memory coupled to the above CPU local bus through core logic, a frame buffer memory coupled to the display controller via a peripheral local bus (e.g., PCI), peripheral circuitry (e.g., clock drivers and signal converters, display driver circuitry), and a display unit.

The CPU is the system master and generally provides overall system control in conjunction with the software operating system. Among other things, the CPU communicates with the system memory holding instructions and data necessary for program execution, normally through core logic. Typically, the core logic is two to seven chips, with one or more chips being "address intensive" and one or more other chips being "data path intensive." The CPU also, in response to user commands and program instructions, controls the contents of the graphics images to be displayed on the display unit via the display controller.

The display controller, which may be, for example, a video graphics architecture (VGA) controller, generally interfaces the CPU and the display driver circuitry, manages the exchange of graphics and/or video data between the frame buffer and the CPU and display during display data update and screen refresh operations, controls frame buffer memory operations, and performs additional basic processing on the subject graphics or video data. For example, the display controller may also include the capability of performing operations such as line draws and polygon

fills. The display controller is for the most part a slave to the CPU.

Generally, the CPU itself provides the display data necessary to update the display screen when a change in the displayed images (data) is required. Due to overhead constraints on the CPU, (as well as bandwidth limitations on PCI local bus or other buses) and limits on the size of the display controller write buffer, the updated display data is generated and stored in the system memory. When the display write buffer has capacity and CPU time is available, the CPU then reads the required information (typically both addresses to the frame buffer and pixel data) from the system memory via the core logic and the CPU local bus and then writes that data via the core logic and PCI local bus into the write buffer of the display controller. Multiple CPU cycles (i.e., a read and a write cycle) are required to write each word of data to the display controller during a display update. This creates serious disadvantages when the efficient use of CPU cycles is critical to higher processing speeds and expanded performance not to mention freeing up the PCI (local) bus for other operations. Display update speed is also limited by the depth of the write buffer on the controller and the bandwidth of the PCI local bus.

Another problem, typically found in the conventional processing/display system architectures discussed above, is unused memory space. Currently, the typical system memory is 4 to 8 megabytes in size. In the foreseeable future, system memories may grow in size to as much as 16 megabytes as new operating systems are developed. In conventional personal computers, system memory, also known as the main memory, is normally constructed from dynamic random access memory devices (DRAMs). Commercial DRAMs are

constructed only in quadrupling densities (i.e., 256KB, 1MB, 4MB) and the maximum size of each addressable storage location is 16 bits wide. Thus, multiple chips are normally required to construct the system memory (which needs to be 64 to 72 bits wide for today's PC systems), although the full capacity of each individual device may not be used. For example, to support a 64-bit wide data bus, 4 parallel "by 16" devices are required per bank. Depending on whether 256KByte or 1MByte devices are used, each bank would have a corresponding capacity of 1MBytes or 4MBytes respectively. If intermediate capacities are required per bank, for example 3MBytes, the larger incrementation must be selected and some memory will go unused. This problem is compounded by the fact that the use of the system memory space is also suboptimal, since the CPU, for operating efficiency, does not necessarily store data contiguously in memory.

Suboptimal use of memory space is also found in the typical frame buffer construction. While the frame buffer normally does not need to be large (typically within the range of 0.8 to 1.25 megabytes), it does need to be "wide" to support display refresh bandwidth requirements. For example, assume that the frame buffer is supporting a 64-bit wide data bus to the display controller. To support such a bus, 4 parallel "by 16" DRAMs are required. If conventional 256k by 16 DRAMs are used, the frame buffer will have a total capacity of 2 megabytes. Thus, even with the largest frame buffers (i.e., 1.25 megabytes) substantial amounts of memory space remain unused.

Thus, the need has arisen for improved apparatus, systems, and methods for more efficiently constructing and managing memory in processing and display systems. In particular, the need has arisen for techniques to

conserve CPU operating cycles during display updates. Advantageously, such techniques would free the CPU to perform other critical operations and thus improve overall system performance. Additionally, the need has arisen for circuits, systems and methods for more efficiently constructing and managing the system and frame buffer memories required in display processing systems. Specifically, such apparatus systems and methods should minimize the number of devices required to construct such memories. As a result, more compact, inexpensive and efficient system architectures can be implemented. These memories, specifically DRAMs, could be multiplexed address/RAS-CAS type systems, or multiple clock/synchronous DRAMs (now under consideration in the industry) or synchronous graphics DRAMs, or DRAMs with special interfaces.

## SUMMARY OF THE INVENTION

The foregoing has outlined rather broadly the features and technical advantages of the present invention in order that the detailed description of the invention that follows may be better understood. Additional features and advantages of the invention will be described hereinafter which form the subject of the claims of the invention. It should be appreciated by those skilled in the art that the conception and the specific embodiment disclosed may be readily utilized as a basis for modifying or designing other structures for carrying out the same purposes of the present invention. It should also be realized by those skilled in the art that such equivalent constructions do not depart from the spirit and scope of the invention as set forth in the appended claims.

According to the principles of the present invention, a processing system is disclosed which includes a unified system/frame buffer memory system. In the unified memory system, both the frame buffer and system memory are collocated in a single integrated circuit or bank of integrated circuits. This is in contrast to the presently-available display control systems where the frame buffer is separate and apart from the system memory and must interface with the remainder of the system through the display controller. According to the principles of the present invention, the frame buffer area of the unified memory includes at least 2 physical memory blocks. One block is used for screen refresh by either the display controller or the CPU. The second block is used for display data update. Advantageously, the system CPU can update data in the update frame buffer block by directly writing to the desired locations. Further, these updates can be made

to the update buffer while the refresh buffer is providing data for refresh of its display screen. This is in contrast to presently available systems where to perform an update, the CPU must first store/retrieve the update data in the system memory, read that data from the system memory and then write that data to the display controller write buffer. Not only do the principles of the present invention conserve valuable system operating cycles, but also allow for the elimination of the write buffer on the display controller, since reads can be made directly from the refresh buffer.

According to a first embodiment of the principles of the present invention, a processing system is disclosed which includes a unified system memory having a system memory area and a plurality of frame buffer memory areas. The processing system further includes a central processing unit, the unified memory lying within an address space of the central processing unit. The central processing unit is operable to update display data in a first selected one of the frame buffer areas while display data from a second selected one of the frame buffer areas provides data for refresh of a display screen of an associated display device.

According to a second embodiment of the present invention, a processing system is provided which includes a unified memory including at least one system memory space and first and second frame buffer spaces. Circuitry is provided as part of the processing system for updating display data stored in the first frame buffer space. Circuitry is also provided for retrieving display data stored in the second frame buffer space for generating a corresponding display substantially concurrent with the updating of the display data stored in the first frame buffer space.

Additionally, the processing system includes circuitry for retrieving display data stored in the first frame buffer space for generating a corresponding updated display.

An additional processing system embodies the present invention. The processing system includes the central processing unit, a CPU local bus coupled to the central processing unit, core logic coupled to the CPU local bus, a display controller coupled to the core logic and the above bus and a unified memory system, coupled to the core logic, the unified memory providing a system memory area and a plurality of frame buffer areas.

The principles of the present invention are also embodied in memory management methods. In one such method, a unified memory is partitioned into a system memory and first and second frame buffer memories. Display data stored in the first frame buffer is updated while display data stored in the second frame buffer is used for generating a corresponding display. Upon completion of the updating of data in the first frame buffer, the data stored in the first frame buffer is retrieved for generating a corresponding updated display.

Systems embodying principles of the present invention have substantial advantages over those of the prior art. In particular, such principle can save CPU operating cycles during display updates freeing the CPU to perform other critical operations and thus improving overall system performance. Additionally, the unified system memory of the present invention allows for the more efficient construction and operation of the memory spaces required in a processing/display system. In particular, by collocating the system memory and frame buffer memory, unused memory space can be minimized and

consequently more compact, inexpensive, and efficient systems can be implemented.

Although the present PC systems do not involve a direct communication between CPU local bus and graphics controller (all the communications between CPU and graphics controller, today, are through PCI local bus only), in future, this will change. When processors like P6 (Intel) add graphics/video/NSP audio functions, there will be a need for direct communication between CPU and graphics controller through CPU local bus. This is similar to a "multitasking" situation.

## BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present invention, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

FIGURE 1 is a functional block diagram of a portion of a processing system responsible for the generation and control of display data according to the principles of the present invention;

FIGURE 2 is a functional block diagram of one possible construction of the unified memory depicted in FIGURE 1; and

FIGURE 3 is a functional block diagram of an integrated display controller/unified memory device suitable in one application in the system of FIGURE 1.

## DETAILED DESCRIPTION OF THE INVENTION

The principles of the present invention and their advantages are best understood by referring to the illustrated embodiment depicted in FIGURES 1-3 of the drawings, in which like numbers designate like parts.

FIGURE 1 is a high level functional block diagram of the portion of a processing system 100 controlling the display of graphics and/or video data. System 100 includes a central processing unit 101, a CPU local bus 102, core logic 103, a display controller 104, a unified system/display memory 105, a digital to analog converter (DAC) 106 and a display device 107.

CPU 101 is the "master" which controls the overall operation of system 100. Among other things, CPU 101 performs various data processing functions and determines the content of the graphics data to be displayed on display unit 107 in response to user commands and/or the execution of application software. CPU 101 may be for example a general purpose microprocessor, such as an Intel Pentium class microprocessor or the like, used in commercial personal computers. CPU 101 communicates with the remainder of system 100 via CPU local bus 102, which may be for example a special bus, or a general bus (common in the industry).

Memory 105 is a "unified" memory system since the system memory and frame buffer are collocated in a single integrated circuit or bank of integrated circuits. This is in contrast to the prior art systems discussed above where the frame buffer is separate and apart from the system memory and interfaces with the remainder of the system through the display controller.

Core logic 103, under the direction of CPU 101, controls the exchange of data, addresses, and

instructions between CPU 101, display controller 104, and unified memory 105. Core logic 103 may be any one of a number of commercially available core logic chip sets designed for compatibility with the remainder of the system, and in particular with CPU 101. One or more core logic chips, such as chip 112 in the illustrated system, are typically "address intensive" while one or more core logic chips, such as chip 114 in FIGURE 1, are "data intensive." CPU 101 can directly communicate with core logic 103 or through an external (L2) cache 115. It should be noted that CPU 101 can also include on-board (L1) cache. L2 cache 115 may be for example a 256KByte fast SRAM device(s).

Display controller 104 may be any one of a number of commercially available VGA display controllers. Display controller 104 may receive data, instructions and/or addresses from CPU 101 either through core logic 103 or directly from CPU 101 through CPU local bus 102. Data, instructions, and addresses are exchanged between display controller 104 and unified memory 105 through core logic 103. Further, addresses and instructions may be exchanged between core logic 103 and display controller 104 via a local bus which may be for example a PCI local bus. Generally, display controller 104 controls screen refresh, executes a limited number of graphics functions such as line draws, polygon fills, color space conversion, display data interpolation and zooming, and video streaming and handles other ministerial chores such as power management. Video data may be directly input into display controller 104.

Digital to analog converter 106 receives digital data from controller 104 and outputs the analog data to drive display 107 in response. In the illustrated embodiment, DAC 106 is integrated with display controller 104 onto a single chip. Depending on the

specific implementation of system 100, DAC 106 may also include a color palette, YUV to RGB format conversion circuitry, and/or X- and Y- zooming circuitry, to name a few options. Display 107 may be for example a CRT unit, a liquid crystal display, electroluminescent display, plasma display, or other type of display device which displays images on a screen as a plurality of pixels. It should also be noted that in alternate embodiments, "display" 107 may be another type of output device such as a laser printer or similar document view/print appliance.

According to the principles of the present invention, unified memory 105 embodies both a system memory 109 and the display frame buffer, which is divided into frame buffer block A 110 and frame buffer block B 111. System memory 109 is preferably a traditional system memory which stores data, addresses, and instructions under the command of CPU 101 as required for executing various processing functions and applications programs. The dual block frame buffer 110/111 resides in the same CPU address space as system memory 109. Preferably, each frame buffer block 110 and 111 is assigned a contiguous block (set) of addresses within the address space of CPU 101, although the address blocks assigned to the two banks may or may not be contiguous with each other. It should also be noted that the addresses allotted frame buffer banks A and B may change depending on the partitioning of unified memory 105 by the operating system being executed by CPU 101. Each frame buffer block 110 and 111 maps pixel by pixel to the screen of display 107 as is done in a conventional frame buffer.

During display generation and update, each frame buffer bank 110/111 maintains the pixel data corresponding to a display screen. One memory bank

110/111 is the "display memory" or "refresh memory" which the display controller 104 accesses (using addresses generated by display controller 104) to refresh the screen on display 107. CPU 101 may also directly access the frame buffer bank 110/111 currently acting as the display memory and refresh the screen of display 107 itself. In this case, display controller 104 would either be bypassed or would simply act as a pipeline for the pixel data being sent to DAC 106 and display 107. Advantageously, all the display data is in one contiguous "refresh block" in the refresh memory which allows the display controller to access the refresh data stored therein with minimal intervention of CPU 101 (if the display data were to be stored in non-contiguous areas of the memory, more CPU intervention would be required to "direct" the display controller to the data.) Since 75% of all display processing time is normally used for screen refresh, the ability to shift the display refresh to the display controller can substantially improve system performance as the CPU 101 is made available for other tasks.

At the same time, the other frame buffer bank 110/111 is used exclusively for screen update. CPU 101 updates the display data within the refresh frame buffer block 110/111 by directly writing to the locations holding the data being modified. The prior art multiple step process of writing to the system memory, reading from the system memory when the display controller write buffer is available, and then writing to frame buffer is thereby reduced to a series of direct write operations to the frame buffer update block. Thus, the update of each word of pixel data within the "screen update" bank is performed using only one CPU cycle for each word of data being updated (depending on such factors as the width of the data bus

and/or number of bits of data CPU 101 can write to unified memory 105 at one time, each word being modified can represent one or more pixels). In other words, if a number of words of data are being updated in the update frame buffer bank, the number of CPU clock cycles which are required to perform the screen update is essentially halved.

Once the screen update is complete, the frame buffer bank 110/111 currently acting as the display memory and the frame buffer bank 110/111 currently acting as the screen refresh memory reverse roles. For example, if block A was being used to refresh the screen while updates to the display were being implemented through writes to block B, when the update to block B is complete, block A becomes the update block and bank B becomes the screen update block.

In a system such as system 100 embodying the principles of the present invention, the display controller write buffers can even be eliminated. Display refresh in this instance may be performed by simply retrieving data directly from the refresh frame buffer block 110/111, and pipelined through display controller 104 towards display unit 107. In this case the refresh buffer essentially replaces the display controller write buffer.

Unified system/frame buffer memory 105 may either be constructed as a monolithic chip or as a multiple chip (device) subsystem. Such a subsystem 200 is illustrated in FIGURE 2. System 200 is comprised of a plurality of memory banks 201. When used in system 100, each bank 201a is coupled to core logic 103 by an address bus 202, a data bus 203, and a control bus 204. Banks 201 may operate in a non-multiplexed addressing scheme with address bus 202 simultaneously presenting both column and row address bits to banks 201.

Alternatively, banks 201 may operate in a multiplexed (RAS/CAS) scheme, as well as "synchronous DRAM schemes" (a synchronous clock, in addition to RAS and CAS), with row and column address multiplexed on address bus 202. Control bus 204 carries the conventional DRAM control signals (such as RAS and CAS) in a multiplexed address scheme, output enable, and read/write. As discussed further below, each bank 201 is associated with a separate set and bank selection is a function of the addresses presented on address bus 202.

In the application of unified system/frame buffer memory 105, one bank 201 may be used for frame buffer block A, a second bank 201 used for frame buffer block B and the remaining banks 201 used for system memory 109. Assume for discussion purposes that unified memory 105 is an 8-megabyte (64-megabit) memory suitable for supporting a state of the art operating system such as Microsoft Windows 95. In this example, each bank 201 is a 1-megabyte DRAM device. In order to perform a 1-bit out of 64-megabit selection (i.e. a "by 1" device is being used), 26 address bits are required in a non-multiplexed scheme. If each bank is constructed as a by 4, by 8, by 16, by 32, or by 64-bit device, then the number of address bits is appropriately reduced. For the by 1-bit device, 3 bits of each address word (for example, the 3 least significant bits) are used for bank select. To address either frame buffer block A, frame buffer block B or the system memory, CPU 101 simply modifies these 3 address bits.

FIGURE 3 is a functional block diagram of an alternate processing system 300. In system 300, display controller 104 and DAC 106 have been integrated along with system memory 105 and a plurality of frame buffer blocks onto a single chip monolithic integrated

circuit 301. Display controller/DAC 104/106 accesses each frame buffer block through an internal address and data bus 306, which is also used to drive display device 107. As in system 100, CPU 101 can directly write to any frame buffer block to affect a display update. As discussed below, one or more of the other frame buffer blocks can be used to refresh the display screen.

Specifically, a pair of blocks 304A and 304B are provided as memory spaces for a corresponding pair of video frame buffers A and B. Also included on integrated circuit 301 are a pair of blocks 305A and 305B which provide a corresponding pair of graphics frame buffers A and B. As in the case of frame buffer blocks 110 and 111 described above, the video frame buffer blocks 304A and 304B are alternately used as a video update block (buffer) and a video refresh block (buffer). The same is true for buffers 305A and 305B which alternately act as update and refresh blocks (buffers) only for the graphics data. Also provided on integrated circuit 301 is a motion picture expert's group (MPEG) frame buffer 307. Block 307 is dedicated to storing data in the MPEG format and is also within the address base of CPU 101.

Although the present invention and its advantages have been described in detail, it should be understood that various changes, substitutions and alterations can be made herein without departing from the spirit and scope of the invention as defined by the appended claims.

WHAT IS CLAIMED IS:

1. A processing system comprising:

a unified system memory including a system memory area and a plurality of frame buffer memory areas; and

a central processing unit, said unified memory lying within an address space of said central processing unit and wherein said central processing unit is operable to update display data in a first selected one of said frame buffer areas while display data from a second selected one of said frame buffer provides data for refresh of a display screen of an associated display device.

2. The processing system of Claim 1 wherein said CPU is further operable to retrieve said display data from said second frame buffer memory area for refreshing said display screen.

3. The processing system of Claim 1 and further comprising a display controller for interfacing said unified system memory and said display device.

4. The processing system of Claim 1 wherein said display controller is further operable to retrieve said display data from said second frame buffer area for refreshing said display screen.

5. The system of Claim 1 wherein said first and second frame buffer areas each correspond to a contiguous set of addresses within an address space associated with said unified memory.

6. The system of Claim 1 wherein said system memory area corresponds to a contiguous set of addresses within an address space associated with said unified memory.

7. The system of Claim 1 wherein said system memory area corresponds to a plurality of sets of address spaces within an address space associated with said unified memory.

8. The system of Claim 1 wherein each of said memory areas corresponds to a separate contiguous physical memory area.

9. The system of Claim 1 wherein said unified memory is constructed from a plurality of integrated circuit chips.

10. The system of Claim 9 wherein said first and second frame buffer memory areas are each allocated to at least one dedicated integrated circuit chip.

11. A processing system comprising:

a unified memory including at least one system memory space and first and second frame buffer spaces;

circuitry for updating display data stored in the first frame buffer space;

circuitry for retrieving display data stored in the second frame buffer space for generating a corresponding display substantially concurrent with the updating of said display data stored in said first frame buffer space; and

circuitry for retrieving display data stored in the first frame buffer space for generating a corresponding updated display.

12. The processing system of Claim 11 wherein said circuitry for updating said display data stored in said first buffer space comprises a central processing unit.

13. The processing system of Claim 11 wherein said circuitry for retrieving data stored in said first frame buffer space comprises a central processing unit.

14. The processing system of Claim 11 wherein said circuitry for retrieving data stored in said second memory space comprises a central processing unit.

15. The processing system of Claim 11 wherein said circuitry for retrieving data stored in said first memory space comprises a display controller.

16. The processing system of Claim 11 wherein said circuitry for retrieving data stored in said second memory space comprises a display controller.

17. The processing system of Claim 11 wherein said unified memory is constructed on a single integrated circuit chip.

18. A processing system comprising:

a central processing unit;

a bus coupled to said central processing unit;

core logic coupled to said bus;

a display controller coupled to said core logic and said bus; and

a unified memory system coupled to said core logic, said unified memory providing a system memory area, and a plurality of frame buffer areas.

19. The processing system of Claim 18 wherein said CPU is operable to write data to a first one of said frame buffer areas through said system bus and said core logic for display update and read data from a second one of said frame buffer areas for display refresh.

20. The processing system of Claim 18 wherein said CPU is operable to write data to a first one of said frame buffer areas through said system bus and said core logic for display update and said display controller is operable to read data from a second one of said frame buffer areas for display refresh.

21. The processing system of Claim 18 wherein said unified frame buffer is constructed from a plurality of memory devices.

22. The processing system of Claim 21 wherein selected ones of said plurality of memory devices are dedicated to corresponding ones of said memory areas.

23. The processing system of Claim 18 wherein selected ones of said frame buffer areas comprise video frame buffers.

24. The processing system of Claim 18 wherein said ones of said frame buffer areas comprise graphics frame buffers.

25. The processing system of Claim 18 wherein said ones of said frame buffer areas comprise an MPEG frame buffer.

26. A memory management method comprising the steps of:

partitioning a unified memory into a system memory and first and second frame buffer memories;

updating display data stored in the first frame buffer;

during said step of updating, retrieving display data stored in the second frame buffer for generating a corresponding display; and

upon completion of said step of updating, retrieving display data stored in the first frame buffer for generating a corresponding updated display.

27. The method of Claim 26 wherein said step of updating comprises the substep of writing to at least one location in the first frame buffer directly from a CPU.

28. The method of Claim 26 wherein said steps of retrieving comprise the steps of retrieving the display data in response to addresses provided by an associated display controller.

29. The method of Claim 26 wherein said steps of retrieving comprise the steps of retrieving the display data in response to addresses provided from a CPU.

30. The method of Claim 26 wherein said display data includes graphics data.

31. The method of Claim 26 wherein said display data includes video data.

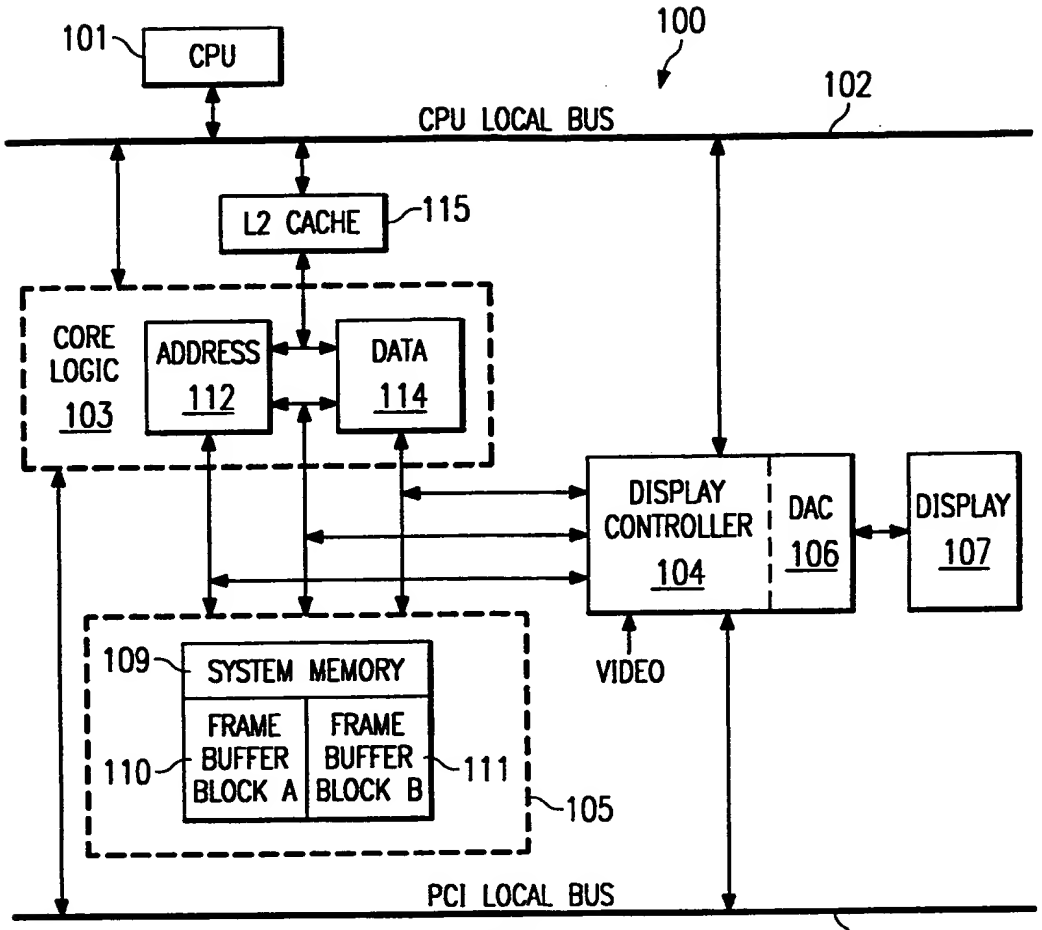
101
CPU
100
102
CPU LOCAL BUS
L2 CACHE
115
CORE LOGIC 103
ADDRESS 112
DATA 114
DISPLAY CONTROLLER 104
DAC 106
DISPLAY 107
109
SYSTEM MEMORY
FRAME BUFFER BLOCK A
FRAME BUFFER BLOCK B
110
111
105
VIDEO
PCI LOCAL BUS
116

*FIG. 1*

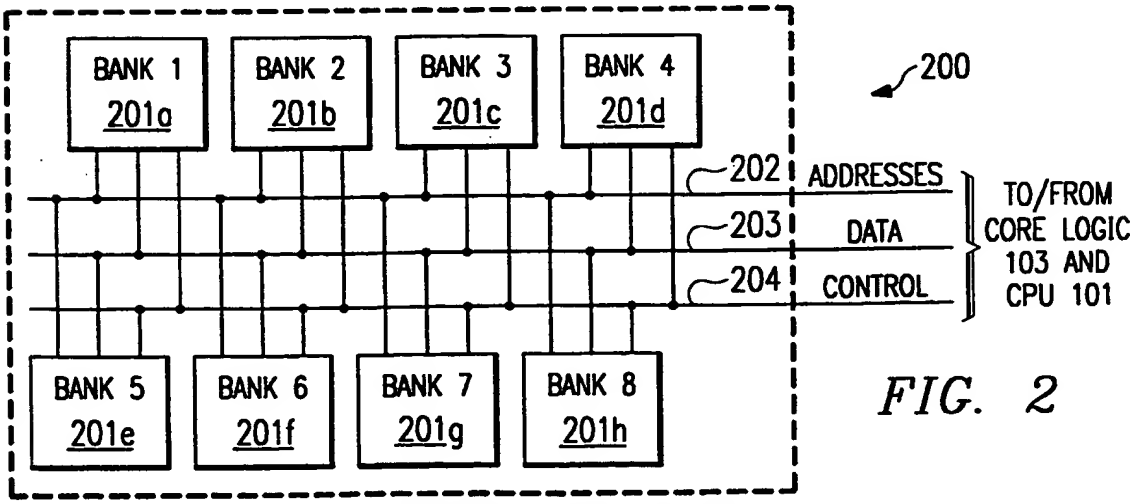
BANK 1 201a
BANK 2 201b
BANK 3 201c
BANK 4 201d
200
202
ADDRESSES
203
DATA
204
CONTROL
TO/FROM CORE LOGIC 103 AND CPU 101
BANK 5 201e
BANK 6 201f
BANK 7 201g
BANK 8 201h

*FIG. 2*

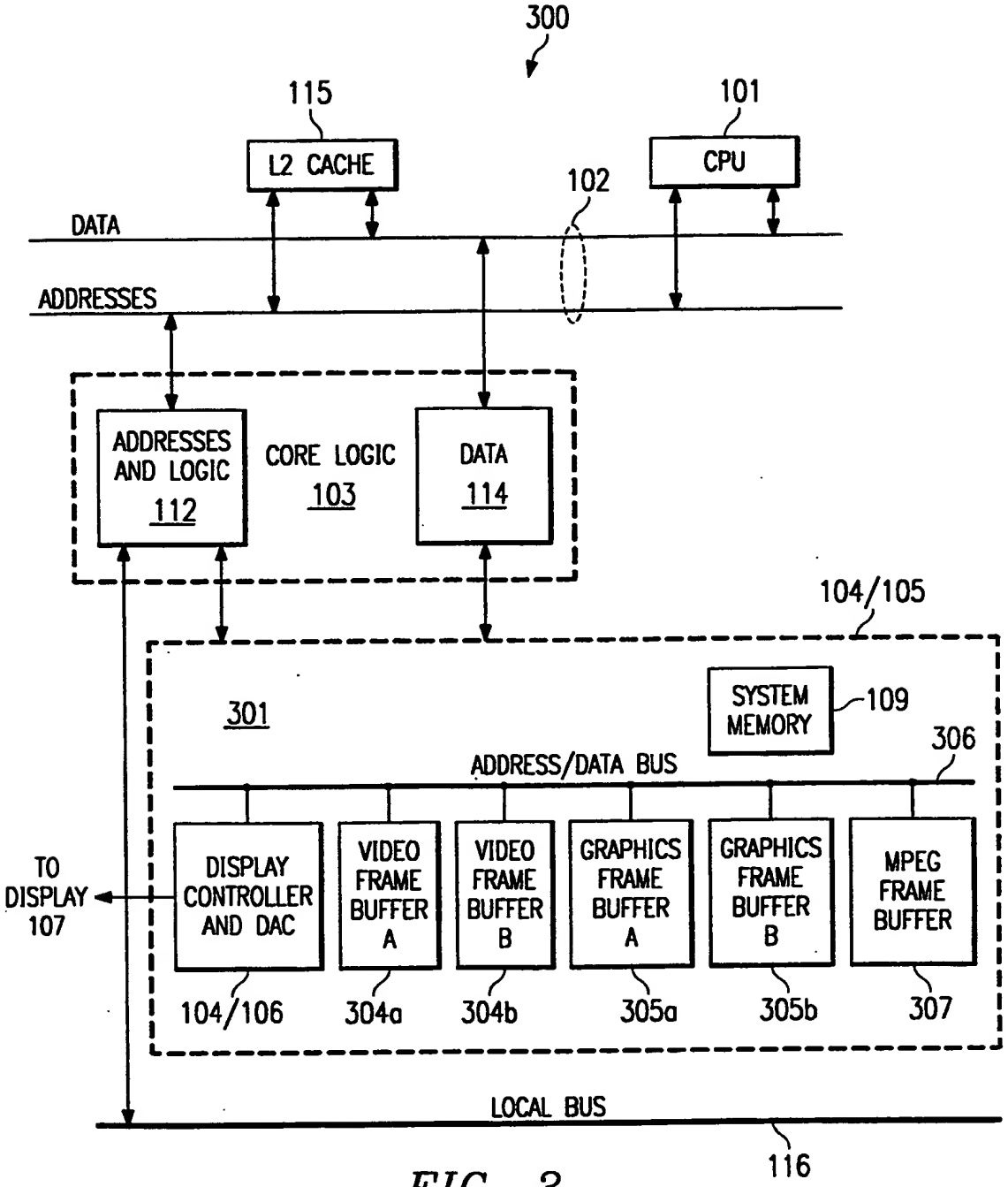
300
115
L2 CACHE
101
CPU
102
DATA
ADDRESSES
ADDRESSES AND LOGIC 112
CORE LOGIC 103
DATA 114
104/105
301
SYSTEM MEMORY
109
306
ADDRESS/DATA BUS
TO DISPLAY 107
DISPLAY CONTROLLER AND DAC
VIDEO FRAME BUFFER A
VIDEO FRAME BUFFER B
GRAPHICS FRAME BUFFER A
GRAPHICS FRAME BUFFER B
MPEG FRAME BUFFER
104/106
304a
304b
305a
305b
307
LOCAL BUS
116

*FIG. 3*

# INTERNATIONAL SEARCH REPORT

Intern· ·al Application No
PCT/US 96/12829

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 G09G1/16

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 G09G

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category * | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| X<br><br>Y | DE,A,35 30 602 (PRÜFTECHNIK DIETER BUSCH + PARTNER GMBH) 5 March 1987<br><br>see Abtsract<br>see column 4, line 65 - column 5, line 19; claim 8; figures 1,4<br>see column 8, line 49 - column 9, line 63<br>see column 10, line 68 - column 11, line 40<br>--- | 1-4, 11-18, 26-28,30<br>5-10,29, 30 |
| Y | EP,A,0 194 092 (COMPUTER GRAPHICS LABORATORIES INC.) 10 September 1986<br>see Abstract<br>see page 41, line 13 - page 50, line 17; figures 11-17<br>---<br>-/-- | 5-8 |

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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"&" document member of the same patent family

| Date of the actual completion of the international search | Date of mailing of the international search report |
|---|---|
| 19 December 1996 | 06. 01. 97 |
| Name and mailing address of the ISA<br>European Patent Office, P.B. 5818 Patentlaan 2<br>NL - 2280 HV Rijswijk<br>Tel. (+31-70) 340-2040, Tx. 31 651 epo nl,<br>Fax: (+31-70) 340-3016 | Authorized officer<br>Corsi, F |

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# INTERNATIONAL SEARCH REPORT

Interr nal Application No
PCT/US 96/12829

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

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| Y | US,A,4 298 957 (DUVALL ET AL.) 3 November 1981<br>see Abstract<br>see column 3, line 18 - column 5, line 16; figures 1-3,6-9,11<br>see column 8, line 33 - column 10, line 45 | 18-24, 29,30 |
| A | EP,A,0 503 956 (C-CUBE MICROSYSTEMS) 16 September 1992<br>see Abstract<br>see page 3, line 10 - line 29<br>see page 6, line 30 - line 43; figures 2,3<br>see page 7, line 2 - line 13<br>see page 8, line 57 - page 9, line 16 | 25 |
| A | EP,A,0 266 506 (I.B.M. CO.) 11 May 1988<br>see Abstract<br>see page 3, line 36 - line 51; figures 1,7<br>see page 4, line 24 - line 45 | 18 |

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Information on patent family members

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PCT/US 96/12829

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